Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended). A timing circuit for generating clock signals, comprising:

~~an~~ a plurality of acquisition digital phase locked loops with a wide capture range for closely following ~~an~~ respective input signals and ~~with its~~ their associated disturbances;

a functional circuit deriving a digital output from the outputs of said acquisition phase locked loops according to a mathematical equation; ~~and~~

an output digital phase locked loop having a slow response relative to said acquisition phase locked loop, said output digital phase locked loop tracking ~~a~~ the digital output of said ~~acquisition phase locked loop~~functional circuit to generate an output signal for the timing circuit; and

wherein said acquisition digital phase locked loop and said output phase locked loop include digital low pass filters, said digital low pass filter in said acquisition digital phase locked loop having a higher cut-off frequency than said digital low pass filter in said output phase locked loop.

2 (canceled)

3 (currently amended). A timing circuit as claimed in claim 1, wherein said digital low pass filter in said acquisition digital phase locked loop has a ~~sufficiently high~~ cut-off frequency high enough to ensure that the output closely tracks the input signal and its associated error components.

4(currently amended). A timing circuit as claimed in claim 3, wherein said digital low pass filter in said output digital phase locked loop has a ~~sufficiently low~~ cut-off frequency low enough to ensure that the output tracks the output of said acquisition digital phase locked loop signal without the associated error components present in the input signal.

5(canceled)

6(canceled).

7(currently amended). A timing circuit as claimed in claim [[6]] 1, wherein said functional circuit is an adder to combine the outputs of said acquisition digital phase locked loops to provide an average.

8(original). A timing circuit as claimed in claim 7, wherein said adder generates a weighted average.

9(canceled).

10(currently amended). A timing circuit as claimed in claim [[5]] 1, wherein the inputs of said acquisition digital phase locked loops are connected through respective multiplexers to a plurality of inputs and a crystal oscillator.

11(currently amended). A method of generating clock signals from ~~an~~ input signals subject to errors, comprising:

tracking the input signals and ~~its~~ their error components with ~~an~~ a plurality of acquisition digital phase locked loops to produce ~~a~~ respective digital outputs ~~signal, and~~;

passing the digital outputs of said acquisition digital phase locked loops through a functional circuit which derives a digital output from the digital outputs of said acquisition phase locked loops according to a mathematical equation;

tracking ~~said~~ the digital output of said functional circuit ~~signal~~ with an output digital phase locked loop with a slow response relative to said acquisition digital phase locked loop so as to eliminate said error components; and

wherein said acquisition digital phase locked loop has a digital filter with a high cut off frequency relative to the cut-off frequency of a digital filter in said output digital phase locked loop.

12(canceled)

13(canceled)

14(canceled).

15(currently amended). A method as claimed in claim ~~13~~11, wherein said functional ~~block~~ circuit combines said digital outputs of said acquisition digital phase locked loops to produce an average.

16(original). A method as claimed in claim 15, wherein said average is a weighted average.

17(currently amended). A method as claimed in claim [[13]] 11, wherein one of a plurality of input signals are selectable for input to each of said acquisition phase locked loops.

18(Currently amended). A method as claimed in claim 17, wherein one of said input signals is derived ~~form~~ from a crystal oscillator for test purposes.

19(currently amended). A method as claimed in claim 11, wherein said filter in said acquisition phase locked loop has a cut-off frequency of a few hundred Hertz.

20(canceled).